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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,005	02/25/2004	Shigeru Fujita	SON-2612/DIV	9742
23353	7590	05/13/2005	EXAMINER	
RADER FISHMAN & GRAUER PLLC			LE, THAO X	
LION BUILDING			ART UNIT	
1233 20TH STREET N.W., SUITE 501			PAPER NUMBER	
WASHINGTON, DC 20036			2814	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/785,005	Applicant(s) FUJITA, SHIGERU	
	Examiner Thao X. Le	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 13-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 13-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 3-4 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pub 2003/0194853 to Jeon.

Regarding claim 1, Jeon discloses a semiconductor device fig. 1 comprising: a semiconductor substrate 102 [0039], a high dielectric-constant film 110a [0043] on the semiconductor substrate 102, and a nitride layer 110d [0023] & [0043] on the high-dielectric-constant film 110a, fig. 6, wherein the high dielectric constant film 110a comprised of enhanced dielectric material of films, fig. 6 including ZrO_2 , HfO_2 [0025] and [0048], film having multiple-layer structure of at least two layers of the enhanced dielectric material of films 110a/110c [0043] fig. 6.

Regarding claim 3, Jeon discloses the semiconductor device according to claim 1, wherein the nitride layer 110d is formed by introducing nitrogen in to the top surface portion of the high-dielectric-constant film 110c [0075].

Regarding claim 4, Jeon discloses the semiconductor device according to claim 1 wherein the semiconductor substrate 102 is a silicon substrate [0039].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2, 5, 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub.2003/0194853 to Jeon in view of US 6436848 to Ramkumar.

Regarding claims 2 and 5, Jeon discloses the semiconductor device according to claim 1, further comprising the gate electrode 108 forming on the nitride layer 110d, fig.

1.

But Jeon does not expressly disclose the boron doping p-type impurity polysilicon layer.

However, Ramkumar discloses a semiconductor device wherein polysilicon gate layer is being doped with boron to form P-type gate, column 1 line 27-30. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the p-type polysilicon gate teaching of Ramkumar with Jeon's layer 108, because it would have created a p-type gate MOSFETS.

Regarding claims 13 and 16, Jeon discloses a semiconductor device in fig. 1 comprising: a semiconductor substrate 102, a gate insulating film 110 on a semiconductor substrate 102, and a gate electrode 108 on the gate insulating film 110, wherein the gate insulating film includes a high-dielectric-constant film 110a and a

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nitride layer 110d, fig. 6, on the high-dielectric-constant film 110c, wherein the high dielectric constant film 110a is selected from film comprised of enhanced dielectric material of films, fig. 6 including ZrO_2 , HfO_2 [0025], and plurality of film having multiple-layer structure of at least two layers of the enhanced dielectric material of films 110a/110c, fig. 6.

But Jeon does not expressly disclose a gate electrode 108 including at least a p-type impurity layer.

However, Ramkumar discloses a semiconductor device wherein polysilicon gate layer is being doped with boron to form P-type gate, column 1 line 27-30. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the p-type polysilicon gate teaching of Ramkumar with Jeon's layer 108, because it would have created a p-type gate MOSFETS.

Regarding claim 14, Jeon discloses the semiconductor device wherein the nitride layer 110d is formed by introducing nitrogen in to the top surface portion of the high-dielectric-constant film 110c [0075].

Regarding claim 15, Jeon discloses the substrate 102 is a silicon substrate [0039].

Response to Arguments

5. Applicant's arguments filed on 28 Mar. 2005 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

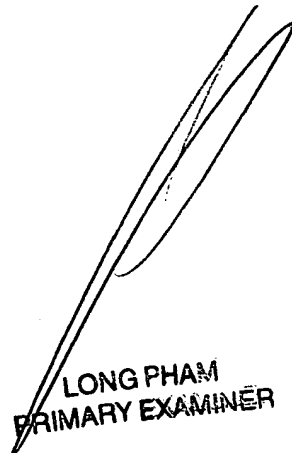
7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
03 May 2005



LONG PHAM
PRIMARY EXAMINER